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Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

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(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
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Power saving method and system

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Power saving method and system

This invention pertains in general to the field of saving energy by reducing the power consumption of electrically powered systems, and more particularly to the reduction of power consumption of electronic mass storage devices, and even more particularly to such a reduction of power consumption in mobile infotainment products.

Mobile storage apparatuses comprise generally mass storage devices, such as Hard Disk Drives (HDD) or optical bit engines. Power consumed by these HDDs or optical bit engines form a significant part of the overall power consumed by such mobile device. As such portable devices, e.g. infotainment devices are run on a limited power source, i.e. a battery, it is desired that the operating time with a fully loaded battery is as long as possible before the battery has to be replaced or recharged. This is one of the reasons that the device should consume as little energy as possible.

One principal solution to save energy when using such a storage device, is to switch off the device, when data is not read or written. However, in this case, data access is very slow, when the storage device starts up again after having been inactive. Alternatively, a storage device has been disclosed in WO01/15161, which has several levels of power consumption modes. The device progressively transitions into lower power consumption modes as time proceeds from the last read or write access to/from the device. However, also this device suffers from the disadvantage of long access times when returning to the full power state from a substantially lower power state, i.e. partial shut-down or shut-down of the storage device.

For audio, video or audio-visual streaming applications, for instance in mobile infotainment devices, such as portable MP3 or DVD players, the total energy consumed can, in addition to the above-mentioned method, be significantly reduced by using a buffer memory and buffering schemes. These schemes exploit the fact that it is more efficient to read or write data in a bursty way with a high transmission bit-rate and subsequently to power down the drive, or alternatively to put the drive in standby mode, for as long as possible.

During the time, in which the drive is powered down or in standby, data is read or written respectively from or to the buffer. An example for this type of buffered data transfer is given in US-B-6,496,915.

To this end, solid state RAM is used to buffer the audio-visual data until it is ready to be further processed, either by being consumed by a decoder in the playback case or by being written to the storage medium in the case of recording. This procedure is independent of the storage medium used, wherein typical storage media are e.g. HDDs, CDs, DVDs, BluRay discs or SFFO (Small Form Factor Optical) discs. However, for the sake of simplicity, the remainder of this description will only deal with HDDs. The total power consumed by such a subsystem is determined by the sum of both the powers consumed by the HDD and the buffering solid state RAM. Although the power consumed by the RAM appears at first sight small compared to the power consumption of disc drives, it is not negligible, especially in the case of DRAMs. Power consumption of the buffer is approximately proportional to the buffer size. Furthermore, the larger the size of the buffer, the less power consumes the disc drive. However, at the same time, the buffer memory's power consumption increases with size. In JP-2000298935, it has been proposed to reduce power consumption of a buffer by providing a hardware buffer solution having a small capacity part for high frequency use and a large capacity part for low frequent use. However, this solution is not flexible, as different bit rates to/from the storage device demand different ratios of the two buffer parts. Furthermore, the number of physical chips and internal banks determines in such a design the power consumption, which is fixed and cannot be further reduced due to the design disclosed in JP-2000298935.

Hence, the object of the invention is to provide an adaptive minimisation of the total power consumption of a subsystem comprising a mass storage device and a buffer memory, without impacting the performance of the subsystem under different operating conditions.

The present invention overcomes the above-identified deficiencies in the art and solves at least the above identified problems by providing a method, an apparatus, and a computer-readable medium for adaptively minimising the total power consumption of a subsystem comprising a mass storage device and a buffer memory, according to the appended patent claims.

The general solution according to the invention is to adaptively modify the characteristics of a buffer memory with regard to operating entities of a subsystem, comprising a mass storage device and the buffer memory, for minimising the power consumption of the subsystem in total, such that the subsystem has an optimally low power consumption for a given set of operating entities of the subsystem.

More particularly, an ideal buffer size is determined, and certain areas of the buffer are shut down, such that optimally low power consumption is achieved for a predetermined performance of the subsystem.

According to aspects of the invention, a method, an apparatus, and a computer-readable medium for adaptively minimising the total power consumption of an apparatus comprising a mass storage device and a buffer memory are disclosed.

The present invention has the advantage over the prior art that it adapts the buffer size with regards to current requirements, thus optimally using the subsystem at a given performance within a wide performance range and with a minimum of energy.

Further objects, features and advantages of the invention will become apparent from the following description of embodiments of the present invention, reference being made to the accompanying drawings, in which

Fig. 1 is a graph illustrating the influence of buffer size on total power consumption of the subsystem;

Fig. 2 is a schematic illustration of a subsystem comprising a mass storage device and a buffer memory;

Fig. 3 is a flow chart of an embodiment of the invention;

Fig. 4 is a schematic illustration of a mobile device according to an embodiment of the invention; and

Fig. 5 is a schematic illustration of a computer-readable medium 5 according to an embodiment of another aspect the invention.

According to an embodiment of one aspect of the invention, the characteristics of the following three entities are in steps of a method 3, as shown in Fig. 3, adaptively determined and modified for minimising the power consumption of a subsystem 2, as shown

in Fig. 2, comprising a mass storage device 21, such as a HDD, and a SDRAM buffer memory 22:

- the HDD 21 or optical bit engine
- the SDRAM scheduling buffers 22
- the bit rate of the audio/video stream 24.

Data stream 23 to/from the HDD to the buffers 22 is generally performed at a fixed rate, wherein the rate is fixed for a given HDD location. The actual speed varies generally with the location on disc due to the constant angular velocity with which data is read from the disc. The actual value may in each case be determined, alternatively an average may be used for a given stream. Furthermore, data rates of Constant Angular Velocity (CAV) optical drives are also location dependent. On the other hand, Constant Linear Velocity (CLV) optical drives have a fixed data rate, which is independent of the disc location, whereby in this case a fixed data rate can be assumed. Moreover, data is read in a bursty manner, as described above. Calculations and verification experiments performed by the inventors have shown that the HDD power consumption asysmptotically reduces to a minimum value determined by the division of the bit-rates of the stream and the maximum throughput of the HDD as a function of the scheduler buffer size. Furthermore, the maximum HDD throughput depends on the disk location, i.e. different zones exist. Outer zones have a higher bit density than inner zones, i.e. a higher bit density results in a higher throughput in a CAV system. On the other hand, the power consumption of the SDRAMs increases generally linearly with increasing SDRAM size. From the literature it is known, that the SDRAM power increases linearly with the SDRAM size. Calculations for existing SDRAM chips also verify this. Note that SDRAM power does not increase with buffer size but with SDRAM size. The buffer size may be smaller than the SDRAM size. Both power consumption of the SDRAMs and of the HDD are plotted in the diagram shown Fig. 1 for a typical drive, wherein typical SDRAM sizes for a video stream of 4 Mbps are shown.

As can be seen in Fig. 1, the overall power consumption is optimum for a particular combination of the three above-mentioned entities at a certain scheduler buffer size.

Furthermore, it is assumed that the power consumption characteristics of the HDD and the SDRAMs is stationary over time, except for wear and tear of the HDD.Slightly varying performance may be easily tracked by measuring the actual data throughput as an alternative to assuming a constant value.

The optimum buffer size for a low bit-rate application, such as playing back music with for instance 128kbps, is different from that of a high bit-rate application like a camcorder recording with e.g. 27Mbps. Thus the optimum buffer size of the subsystem's buffer memory will vary over time with respect to different applications using the subsystem.

In case of multiple simultaneous streams, the sum of the bit-rates of all streams is regarded.

Hence, the subsystem's buffer memory has to have a size sufficiently large, in order to provide low power consumption of the subsystem as a total for high bit-rates. However, this leads to undesired excessive power consumption in low bit-rate applications.

The above-mentioned method, shown in Fig. 3, starts at step 30, when e.g. a HDD scheduler initiates a new stream, whereupon in step 31 the HDD data rate is determined. In step 32 the stream bit-rate to/from the buffer memory is determined, wherein the stream bit-rate is generally the average bit-rate of the stream, but may be variable within certain limits for bit-rate encodings. Subsequently, the optimum buffer size, i.e. the buffer size at the above-described minimum of power consumption of the sub-system, is determined in step 33. This may be performed by e.g. actively varying buffer size and measuring/feeding back power consumption, by calculating the optimum buffer size from a formula or by means of a look-up table. When the optimum buffer size ensuring the lowest power consumption of the subsystem is determined, this optimum buffer size is adjusted in step 34. Subsequently, the subsystem runs with the lowest energy consumption possible for a given streaming bit-rate. Note that in variable bit-rate streams the average bit-rate will vary within a certain range.

According to an embodiment of another aspect of the invention, a mobile device is provided. The mobile device comprises at least one SDRAM IC having a number of internal memory banks. Mobile SDRAMs often have a feature that allows them to selectively switch off some of these memory banks. This is sometimes called Partial Array Self Refresh (PASR).

The disk scheduler, that is responsible for accessing the HDD and the SDRAM buffer, uses knowledge on the HDD and the SDRAM to dynamically determine the optimum memory configuration. More precisely, this act is performed each time a new stream is admitted for streaming. The characteristics of the HDD and SDRAMs are stored in the application. If changes over time are expected, e.g. in case of the HDD, these characteristics may be retrieved from the drive itself, e.g. via a special command that is e.g. based on measurements of the HDD.

Fig. 4 illustrates the current embodiment more detailed. An exemplary subsystem 4 comprises an application device 41, reading or writing data from or to a HDD 48, as indicated by data transmission arrow 49. Data is not transmitted directly from/to the HDD, but by means of a Low-power HDD scheduler 42. Scheduler 42 controls data flows 50, 51 from/to buffer memory chips 43, 44, such as SDRAMs, data flow 52 to/from the HDD and data flow 49 to/from the application 41. The streaming rate of data flow 52 to/from the HDD is fixed and determined by the hardware, wherein the dominant factor is the access speed to the actual medium, which in turn is determined by rotations per minute and/or medium characteristics. Usually the bus connected to the HDD is faster than the actual storage medium. In PCs the hardware interface is usually faster than the HDD. However, in CE applications this might not be the case. Furthermore the scheduler 42 controls which memory banks 45 B1, ... B4 are active. This is done by means of switches 46 having control lines 47 connected to the scheduler 42, i.e. the scheduler 42 determines the configuration of memory banks by switching these memory banks on or off. If the banks are internal, switching may occur by setting a register in the SDRAM. Hence, the only unknown entity at the time of designing the subsystem 4 is the bit-rate of the streams 49, 50 and 51, wherein the total bit-rate depends on the application type or the number of simultaneous streams. Every time the application 41 requests the scheduler 42 to start a new stream, it recalculates the optimum buffer size for that particular configuration of the stream, or of the plurality of streams. Subsequently, the scheduler 42 powers up the optimum memory bank configuration. That means, a number of internal memory banks 45 is activated, ensuring the minimum power consumption, according to the above reasoning with reference to Fig. 1, for the given characteristics of the HDD 48, the SDRAM 43, 44 and the bit-rate of the stream.

Hence, the buffer size is determined in a number of banks/ chips and hence the actual calculated number will be rounded off to an integer number of banks for implementational reasons.

In a dynamic configuration with multiple simultaneous streams, two different situations are distinguished. Firstly, when a new stream is admitted by the scheduler and secondly, a stream is stopped and removed by the scheduler. The first case is achieved by powering up extra memory banks. For the second case, it has to be considered, that memory banks still containing buffered data must not be switched off, as otherwise the data is lost. Therefore, powering off of such a memory bank is e.g. either delayed or the buffered data of that memory bank is moved to another memory bank that will remain powered on after which the first memory bank is powered off.

The scheduler 42 or both the scheduler 42 and the application 41 can be embodied as dedicated circuits 1 ASICs) or one or more programmed microprocessors, thus providing a processing 60 unit that carries out this embodiment of the method according to the invention.

A further embodiment of the invention is illustrated in Fig. 5, which shows a computer-readable medium 5. The computer readable medium 5 is any data storage device that can store data, which can thereafter be read by a computer system. Examples of the computer readable medium include hard drives, network attached storage (NAS), read-only memory, random-access memory, CD-ROMs, CD-Rs, CD-RWs, magnetic tapes, and other optical and non-optical data storage devices. The computer readable medium can also be distributed over a network coupled computer systems so that the computer readable code is stored and executed in a distributed fashion.

A computer-readable medium 5 has embodied thereon a computer program for processing by a computer 55. The computer program comprises a plurality of code segments 56, 57, 58, 59 for adaptively minimising the total power consumption of a subsystem comprising a mass storage device and a buffer memory. By means of the code segments an optimum buffer size for which the power consumption of said subsystem is a minimum for a given streaming bit-rate from said buffer memory is calculated. Furthermore, by means of the code segments, the buffer size of said buffer memory is adjusted to said optimum buffer size, such that the power consumption of said subsystem is minimal. More precisely, when e.g. a HDD scheduler initiates a new stream, code segment 56 determines the HDD data rate. A further code segment 57 determines the stream bit-rate to/from the buffer memory. Subsequently, the optimum buffer size, i.e. the buffer size at the above-described minimum of power consumption of the sub-system, is determined by code segment 58. When the optimum buffer size ensuring the lowest power consumption of the subsystem is determined by code segment 58, this optimum buffer size is adjusted by means of code segment 59. Subsequently, the subsystem runs with the lowest energy consumption possible for a given streaming bit-rate.

Applications and use of the above described method, device and computer-readable medium according to the invention are various and include exemplary fields such as the field of portable devices, for instance digital camcorders, personal digital assistants (PDA), but in addition also other systems comprising the above-mentioned subsystem, where power reduction is important. This is for instance the field of computer servers having a large

number of such subsystems and where it is desired to minimise dissipated heat, which is proportional to the power consumed.

The present invention has been described above with reference to specific embodiments. However, other embodiments than the preferred above are equally possible within the scope of the appended claims, e.g. different mass storage devices than those described above, implementing the above-mentioned method by hardware or software, etc.

Furthermore, the term "comprises/comprising" when used in this specification does not exclude other elements or steps, the terms "a" and "an" do not exclude a plurality and a single processor or other units may fulfil the functions of several of the units or circuits recited in the claims.

CLAIMS:

1. A method for adaptively minimising the total power consumption of an apparatus comprising a subsystem comprising a mass storage device and a buffer memory, said method comprising the steps of

determining an optimum buffer size for which the power consumption of said subsystem is a minimum for a given streaming bit-rate to/from said buffer memory, and

adjusting the buffer size of said buffer memory to said optimum buffer size, such that the power consumption of said subsystem is minimal.

2. The method according to claim 1, wherein said step of adjusting the buffer size comprises switching on memory banks and/or memory ICs of said buffer memory for increasing the size of said buffer memory, and switching off memory banks and/or memory ICs for decreasing said buffer memory.

3. The method according to claims 1 or 2, wherein the storage device is a harddisk drive and the step of determining an optimum buffer size comprises

determining a harddisk drive data rate,

determining the stream bit-rate to/from the buffer memory, and

determining the optimum buffer size having the lowest power consumption at the determined stream bit-rate.

4. The method according to claim 3, wherein said optimum buffer size determination step comprises calculating optimum buffer size from a formula, looking up optimum buffer size in a look-up table, or measuring the minimum power consumption of the subsystem in a feedback loop controlling buffer size.

5. The method according to any of the preceding claims, wherein the optimum buffer memory value is determined by the ratio of the stream bit rate and the disk bit rate giving the duty cycle of the harddisk drive for calculating/estimating the harddisk drive power consumption, which subsequently is used to determine the optimal buffer size.

6. The method according to any of the preceding claims comprising powering up extra memory banks and/or memory ICs when a new stream is admitted.

7. The method according to any of claims 1 to 5, wherein a powering down of a memory bank or IC is either delayed or the buffered data of that memory bank or IC is moved to another memory bank that will remain powered on after which the first bank is shut down immediately, when a stream is stopped and removed.

8. The method according to any of the preceding claims, wherein in case of multiple simultaneous streams, the sum of the bit-rates of all streams is determined.

9. A circuit for retrieving data from a mass storage device via a memory buffer comprising a processing unit conceived to:

- adaptively activate or deactivate areas of said buffer memory in such a manner that total power consumption of a subsystem comprising said storage device and said buffer memory is minimised for a given streaming rate to/from said buffer memory; and
- retrieve the data from the mass storage device.

10. An apparatus comprising a subsystem comprising mass storage device, a buffer memory and the circuit according to claim 9.

11. The apparatus according to claim 10, wherein said buffer memory comprises SDRAM circuits having banks of memory adapted to be independently switched on/off.

12. The apparatus according to claims 10 or 11, wherein a scheduler function executable by the processing unit controls accessing the storage device and the buffer memory.

13. A computer-readable medium having embodied thereon a computer program for processing by a computer, the computer program comprising code segments for adaptively minimising the total power consumption of a subsystem comprising a mass storage device and a buffer memory, wherein

a first code segment determines an optimum buffer size for which the power consumption of said subsystem is a minimum for a given streaming bit-rate from said buffer memory, and

a second code segment adjusts the buffer size of said buffer memory to said optimum buffer size, such that the power consumption of said subsystem is minimal.

ABSTRACT:

The present invention relates to reduction of power consumption of electronic mass storage devices, and more particularly to such a reduction of power consumption in mobile infotainment products. These devices are equipped with a subsystem comprising a mass storage device (48) and a buffer memory (43, 44). The size of the buffer memory (43, 44) is adapted in such a way that optimally low power consumption is achieved. This is accomplished by activating or deactivating memory banks (45) comprised in the buffer memory chips. The amount of memory banks (45) activated is determined by operating characteristics of the subsystem, e.g. a desired bit-rate to be achieved for transmissions to/from the mass storage device (48).

Fig. 4

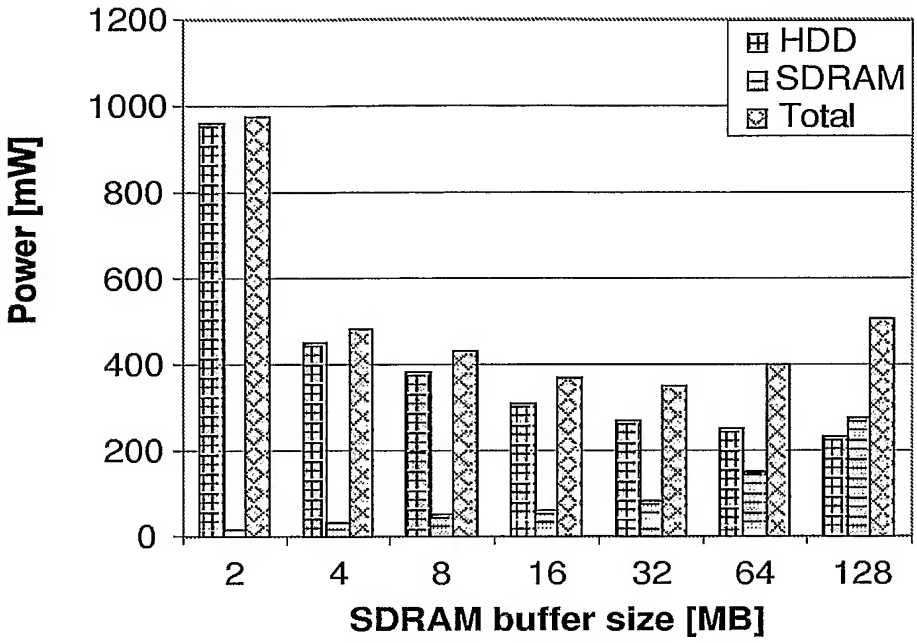
1200
1000
800
600
400
200
0
Power [mW]
HDD
SDRAM
Total
2
4
8
16
32
64
128
SDRAM buffer size [MB]

FIG.1

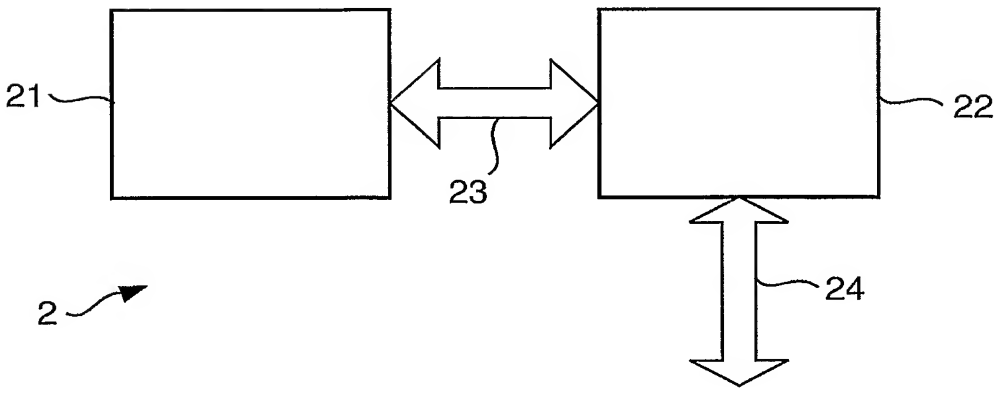
21
22
23
24
2

FIG.2

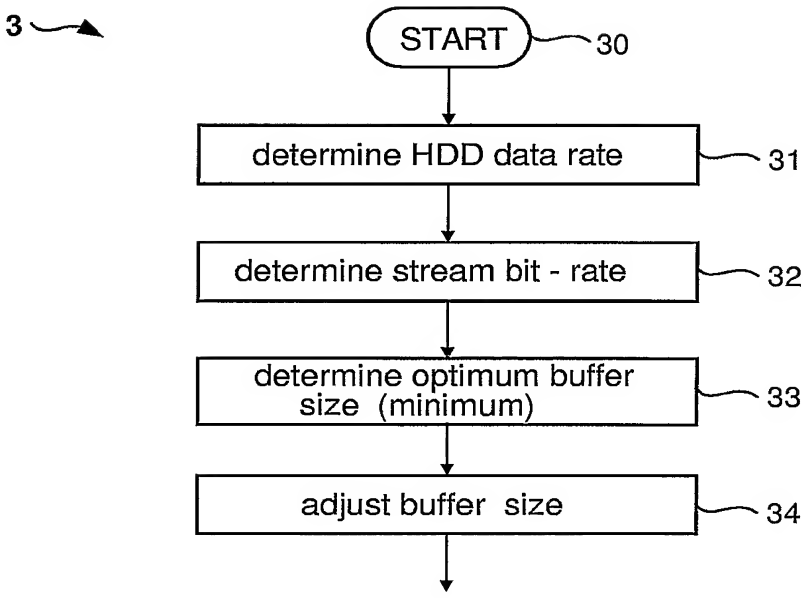
3
START
30
determine HDD data rate
31
determine stream bit - rate
32
determine optimum buffer size (minimum)
33
adjust buffer size
34

FIG.3

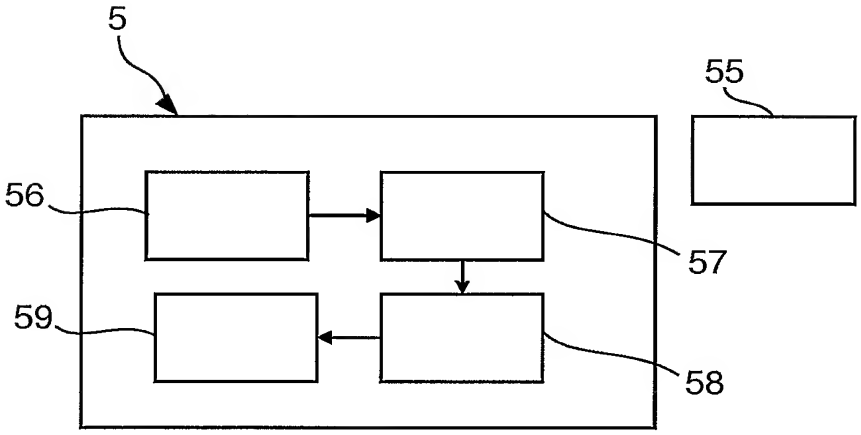
5
55
56
57
59
58

FIG.5

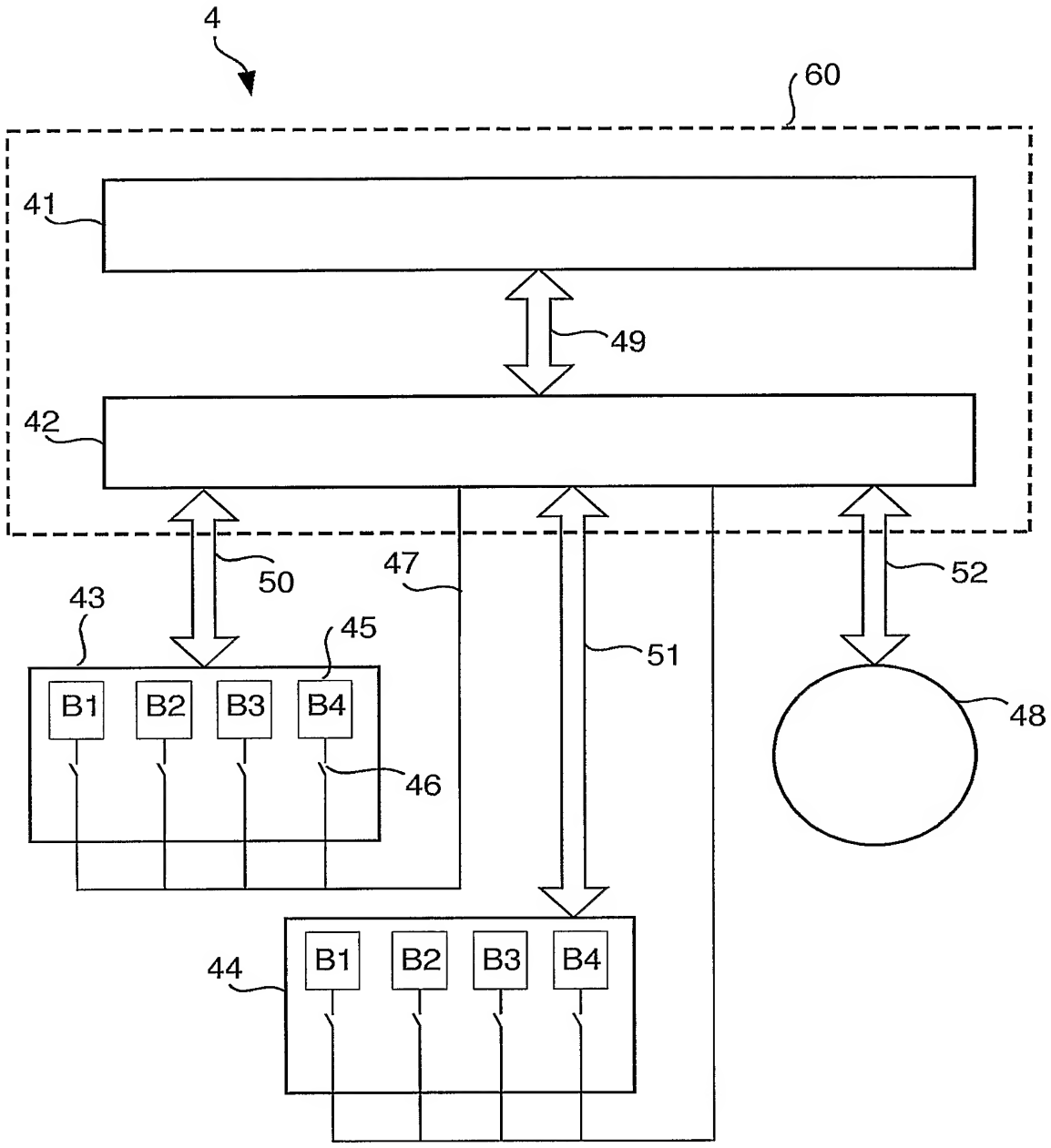

FIG.4